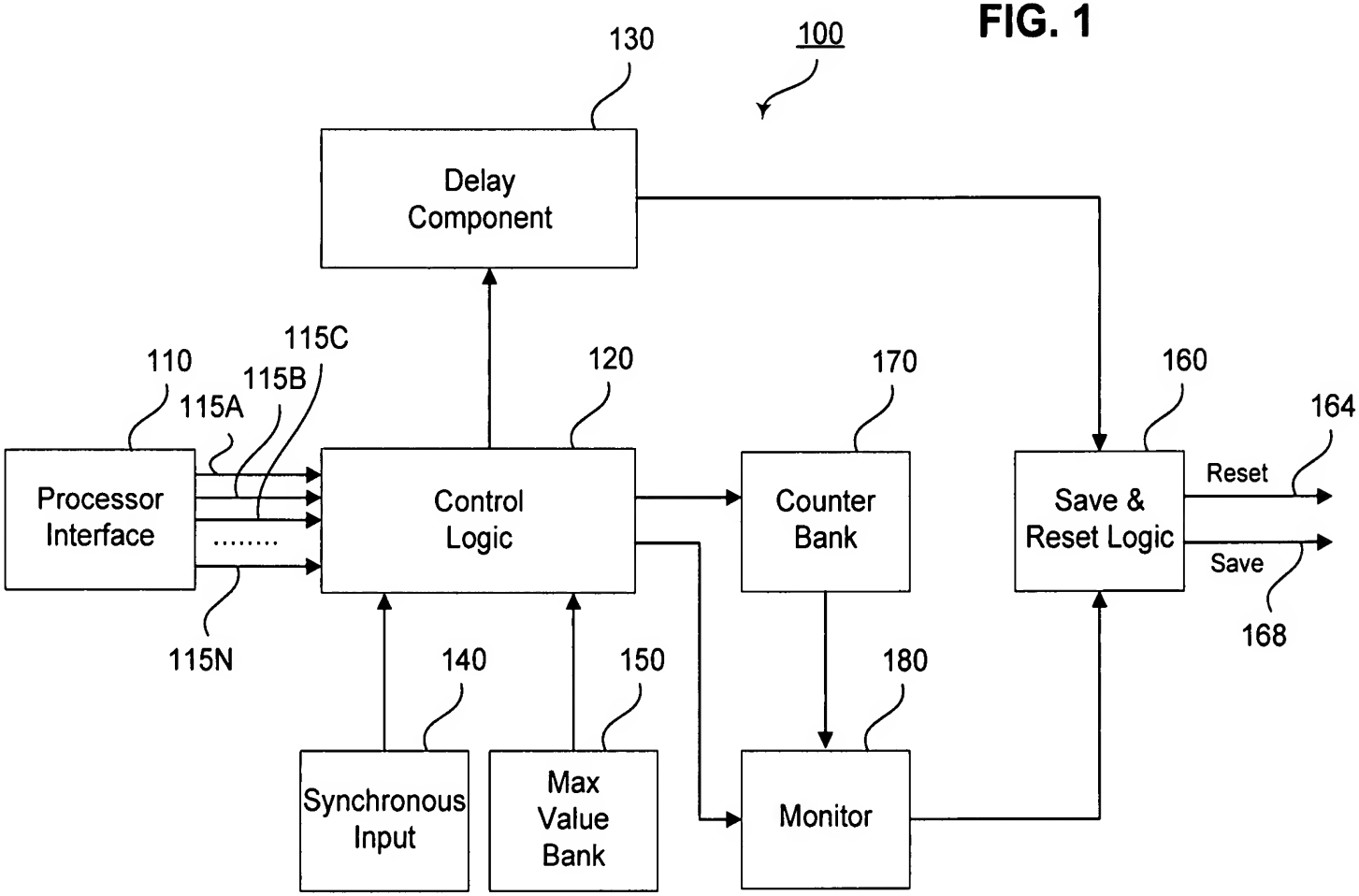
FIG. 1


130
100
Delay Component
110
115A
115B
115C
120
170
160
164
Processor Interface
.....
Control Logic
Counter Bank
Save & Reset Logic
Reset
Save
168
115N
140
150
180
Synchronous Input
Max Value Bank
Monitor

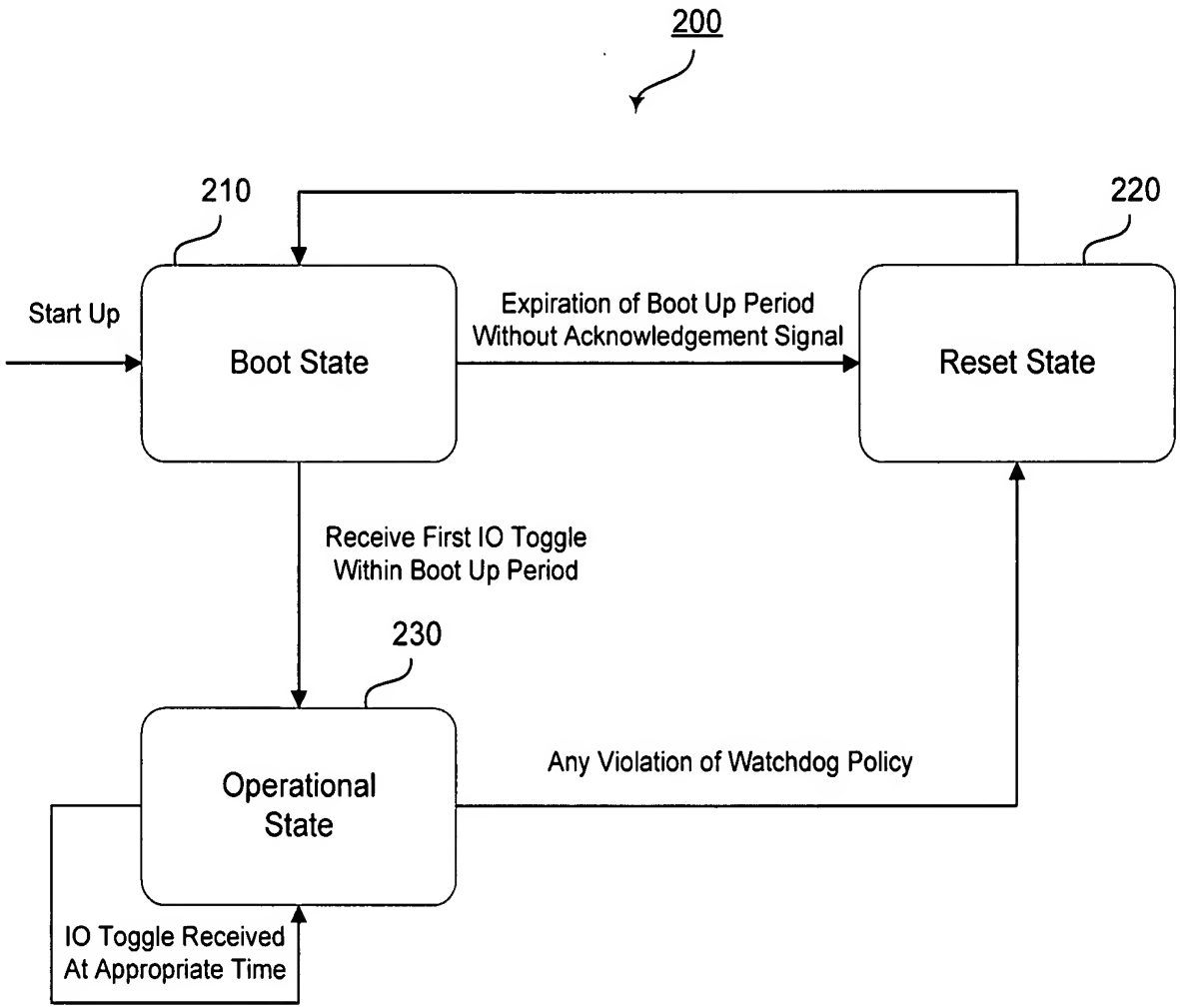
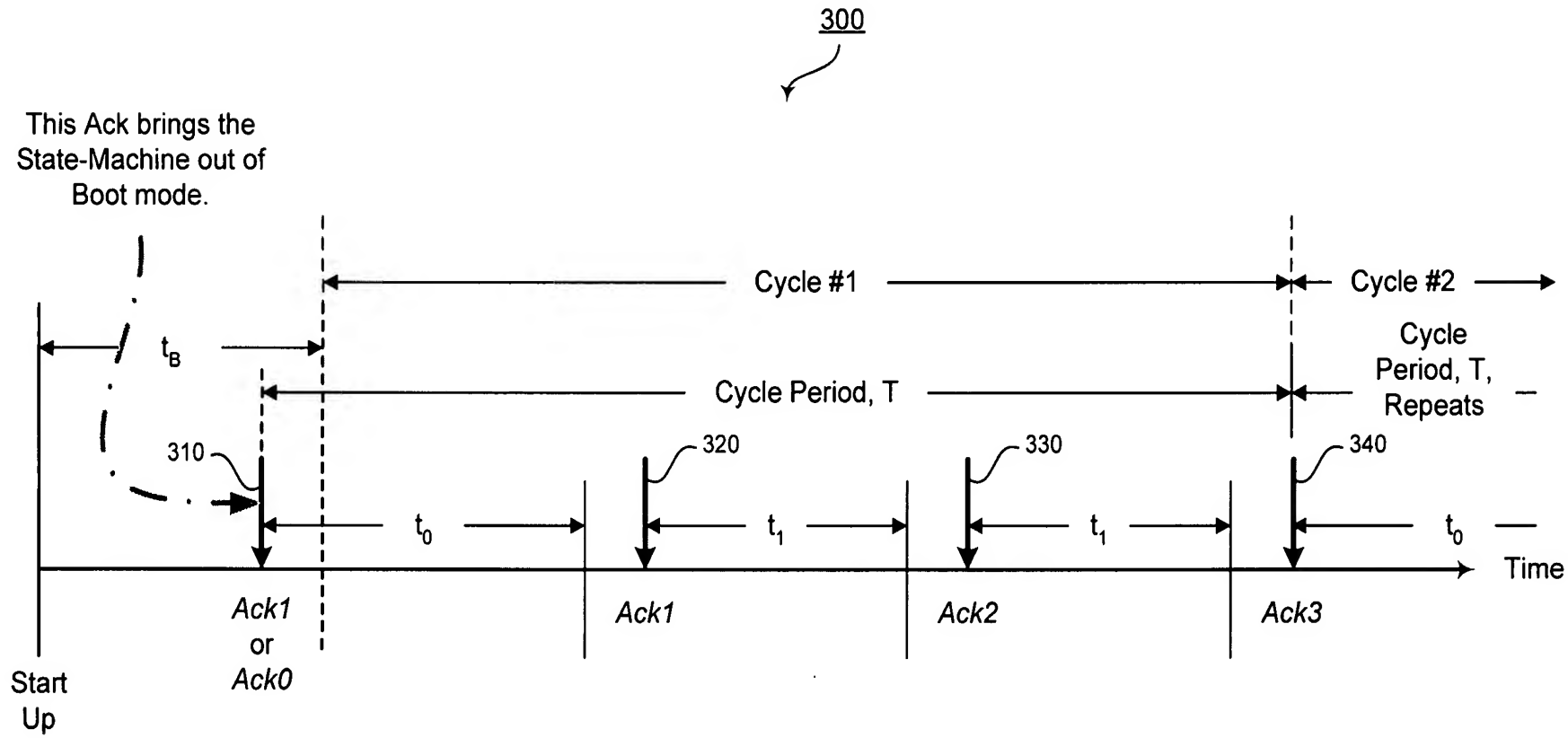

200
210
220
Start Up
Boot State
Expiration of Boot Up Period
Without Acknowledgement Signal
Reset State
Receive First IO Toggle
Within Boot Up Period
230
Operational
State
Any Violation of Watchdog Policy
IO Toggle Received
At Appropriate Time

FIG. 2



Here N =3, and t_B is Boot timer, t_0 is Forbidden Timer, and t_1 is Acknowledgement Timer.

The Sequence of Acks (Ack1, Ack2, and then Ack3) has to be same on every Cycle Period T.

FIG. 3